

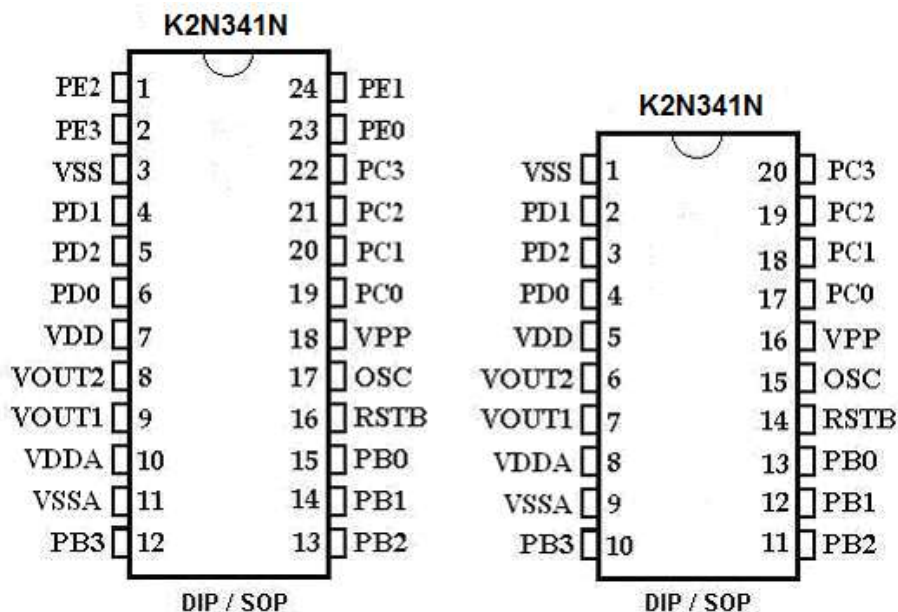


CPU Serial Command

FEATURES

- CPU Serial Command Mode.
- Up to 256 voice groups
- DAC through VOUT2_COUT pin
- PWM through VOUT1 and VOUT2
- Six levels volume control for PWM
- Support 8-bit PCM, 5-bit uLaw and 4-bit ADPCM compression

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Pin Names	Description
VOUT1	PWM output to drive speaker directly.
VOUT2_COUT	PWM output or COUT DAC output select by programmable option.
VSS/VSSA	Power Ground / Analog Power Ground.
OSC	Oscillator input.
VPP	Program power pin, leave during playback.
VDD/VDDA	Positive Power Supply / Analog Positive Power Supply.
PB0	Serial Clock.
PB1	Serial Data.
PB2	System busy output.
PB3	N.C.
PC0, PC1, PC2, PC3	N.C.
PD0, PD1, PD2	N.C.
PE0, PE1, PE2, PE3	N.C.
RSTB	Reset. (Low active)

Pins for programming are: VDD, VDDA, VPP, VSS, VSSA, PB0, PB1, OSC, VOUT2 and RSTB.

CPU Serial Command Mode

The CPU serial mode is designed for CPU interface. The host CPU can send data to control K2N341N. **(PB0) Clock** and **(PB1) Data** are used to input section number. **(PB2) BUSY** is output from the chip to the host CPU for feedback response. Maximum 256 voice section are available.

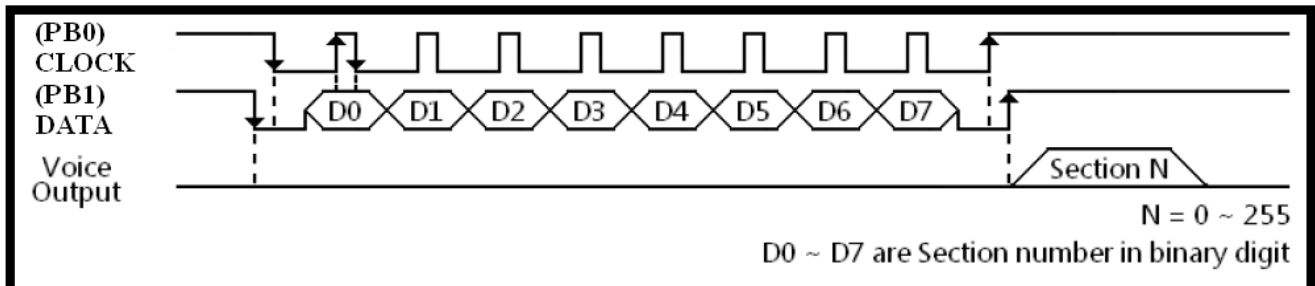


Fig. 1 CPU Serial Command Mode

Ramp-up-down enable or disable

When COUT is used for playback, Ramp-up-down would be enabled. This function eliminates the 'POP' noise at the beginning and end of voice playback.

When VOUT1 and VOUT2 are used to drive speaker directly, the Ramp-up-down is disabled.

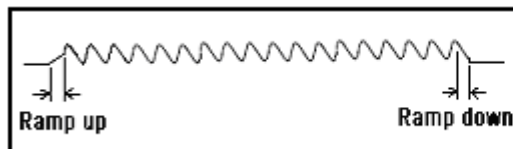


Fig. 1 Ramp-up-down Enable

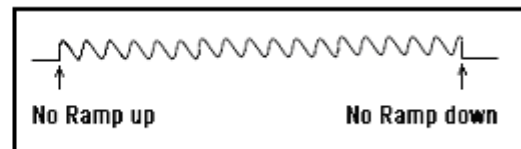
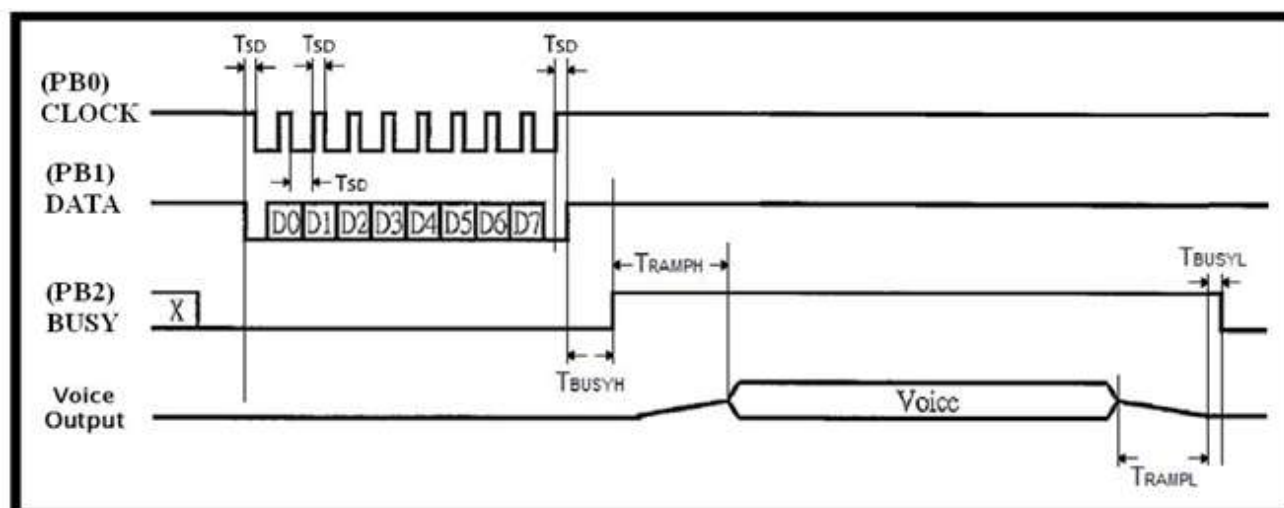


Fig.2 Ramp-up-down Disable



TRIGGER TIMING



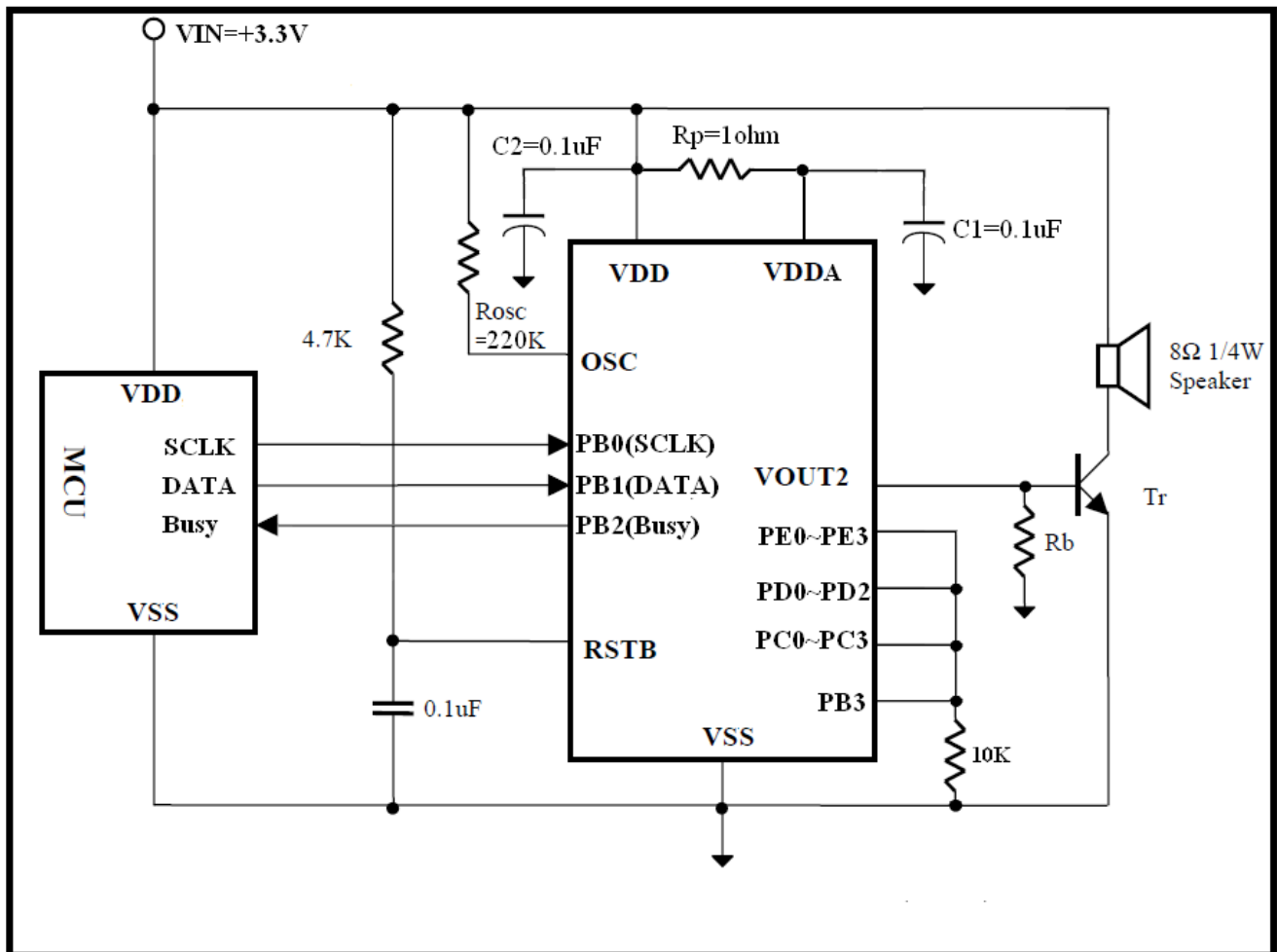
CPU Serial Mode

Symbol	Parameter	Min.	Typ.	Max	Unit
T_{SD}	Serial data stay / hold time	1	—	—	us
T_{RAMPH}	Ramp up time	—	—	64	ms
T_{RAMPL}	Ramp down time	—	—	64	ms
T_{BUSYH}	BUSY output set up time	—	—	1	ms
T_{BUSYL}	BUSY output set down time	—	—	1	ms

Note:

1) Ramp down from the value of the last sound sample. Max. time means ramp down from Voice data equal to FF(hex).

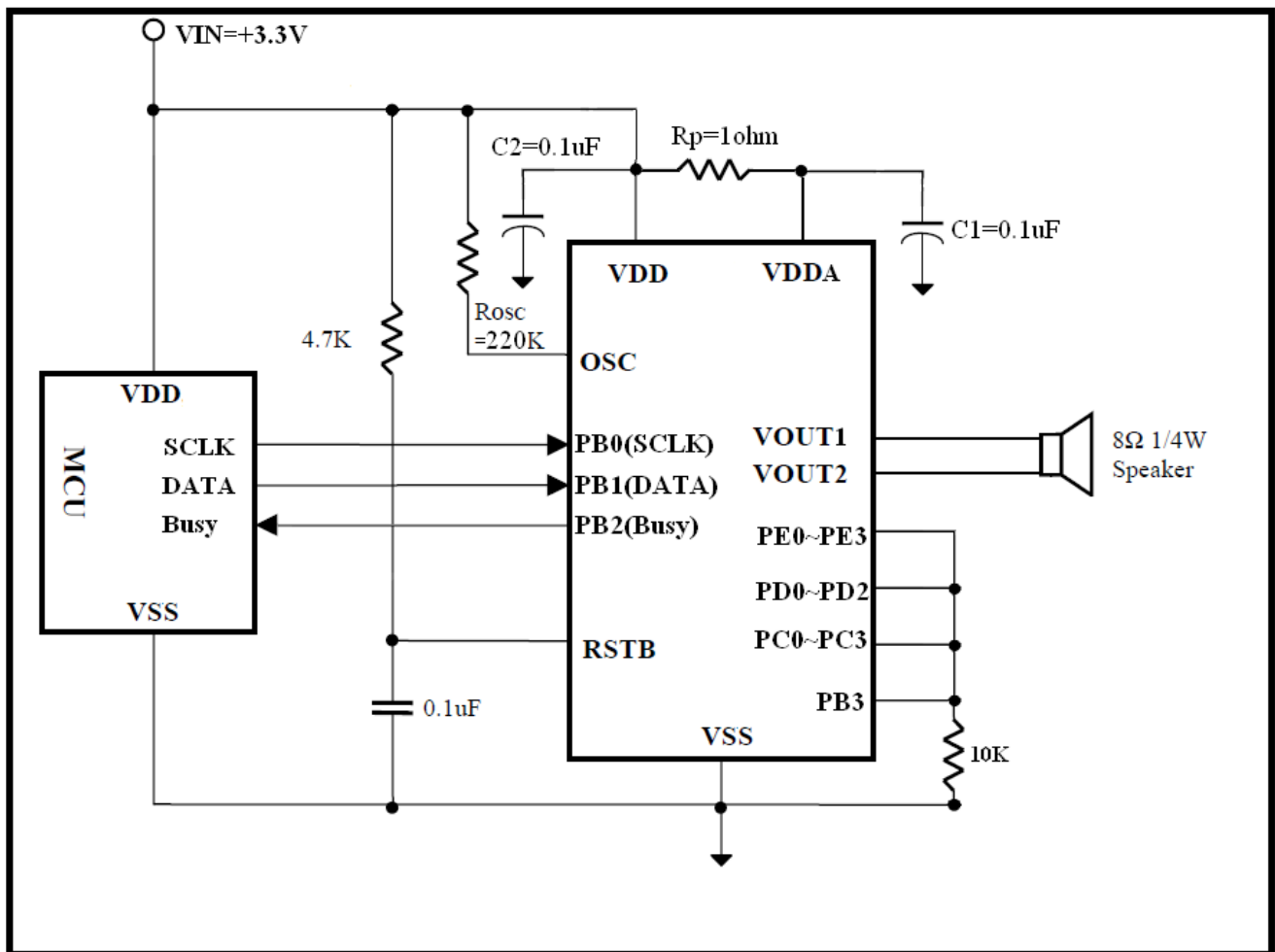
TYPICAL APPLICATIONS



Using 3.3V Supply And CPU Serial Trigger With DAC Driver Speaker

Note

1. PB0 is serial clock pin (input) and it set to internal pull-up.
2. PB1 is serial data pin (input) and it set to internal pull-up.
3. PB2 is busy pin (output).
4. C1 and C2 must be connected as close to the VDD/VDDA and VSS/VSSA pins as possible.
5. $R_{osc} = 220K$ Ohm with $V_{dd}=3.3V$ can support sampling rate up to 14KHz.



Using 3.3V Battery with PWM speaker direct drive

Note

1. PB0 is serial clock pin (input) and it set to internal pull-up.
2. PB1 is serial data pin (input) and it set to internal pull-up.
3. PB2 is busy pin (output).
4. C1 and C2 must be connected directly on the VDD, VDDA and VSS, VSSA pins of the chip.



Bonding Diagrams



Note: Substrate must be connected to VSS

Revision History

Date	Version	Changes
2012-11-21	V1.1	Create.