

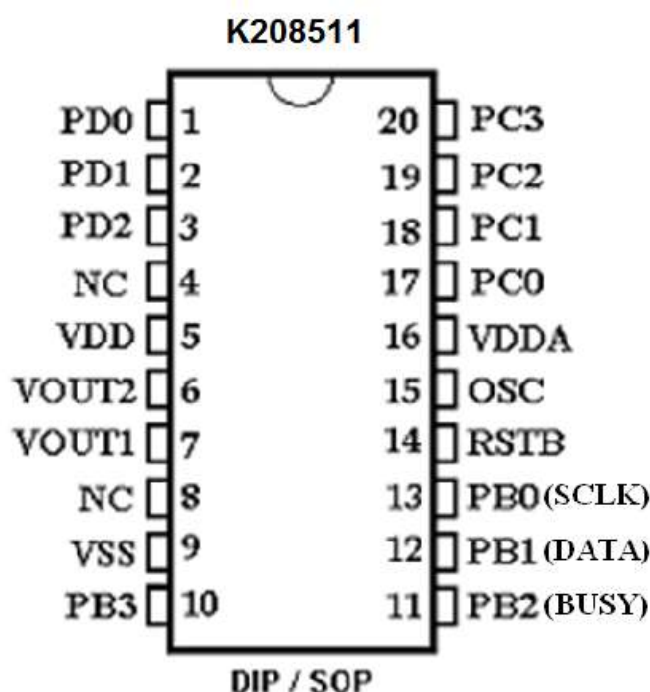


CPU Serial Command

FEATURES

- CPU Serial Command Mode.
- Up to 256 voice groups.
- DAC through VOUT2_COUT pin.
- PWM through VOUT1 and VOUT2.
- Two levels PWM output volume.
- Support 8-bit PCM, 5-bit uLaw and 4-bit ADPCM compression.

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Pin Names	Description
VOUT1	PWM output to drive speaker directly
VOUT2_COUT	PWM output or COUT DAC output select by programmable option
VSS	Power Ground
OSC	Oscillator input
VDDA	Program power pin, connect to VDD during playback
VDD	Positive Power Supply
PB0	Serial Clock pin
PB1	Serial Data pin
PB2	Busy pin
PB3	N.C.
PC0, PC1, PC2, PC3	N.C.
PD0, PD1, PD2	N.C.
RSTB	Reset pin, Low active

Note: pins for memory programming are: VDD, VDDA, VSS, PB0, PB1, OSC, VOUT2 and RSTB.

CPU Serial Command Mode

The CPU serial mode is designed for CPU interface. The host CPU can send data to control K208511. **(PB0) Clock** and **(PB1) Data** are used to input section number. **(PB2) BUSY** is output from the chip to the host CPU for feedback response. Maximum 256 voice section are available.

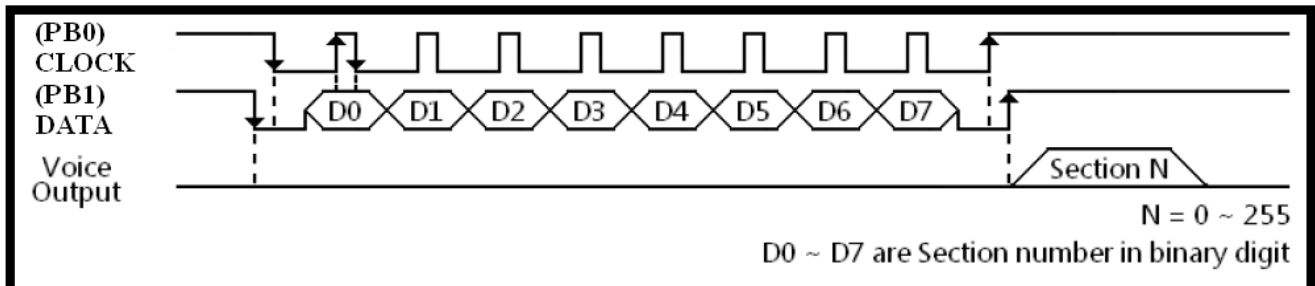


Fig. 1 CPU Serial Command Mode

Ramp-up-down enable or disable

When COUT is used for playback, Ramp-up-down would be enabled. This function eliminates the 'POP' noise at the beginning and end of voice playback.

When VOUT1 and VOUT2 are used to drive speaker directly, the Ramp-up-down is disabled.

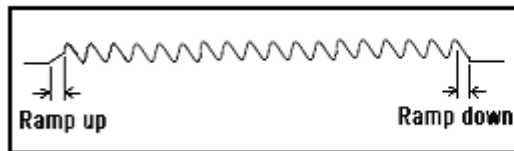


Fig. 2 Ramp-up-down Enable

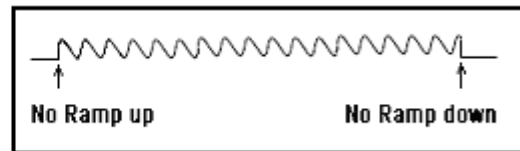
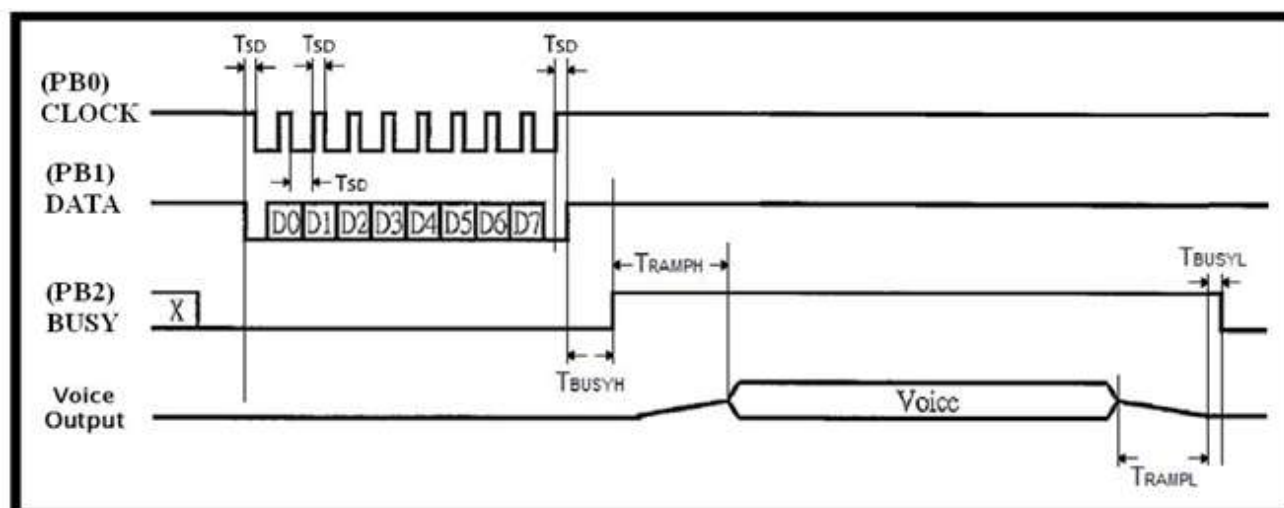


Fig.3 Ramp-up-down Disable

TRIGGER TIMING



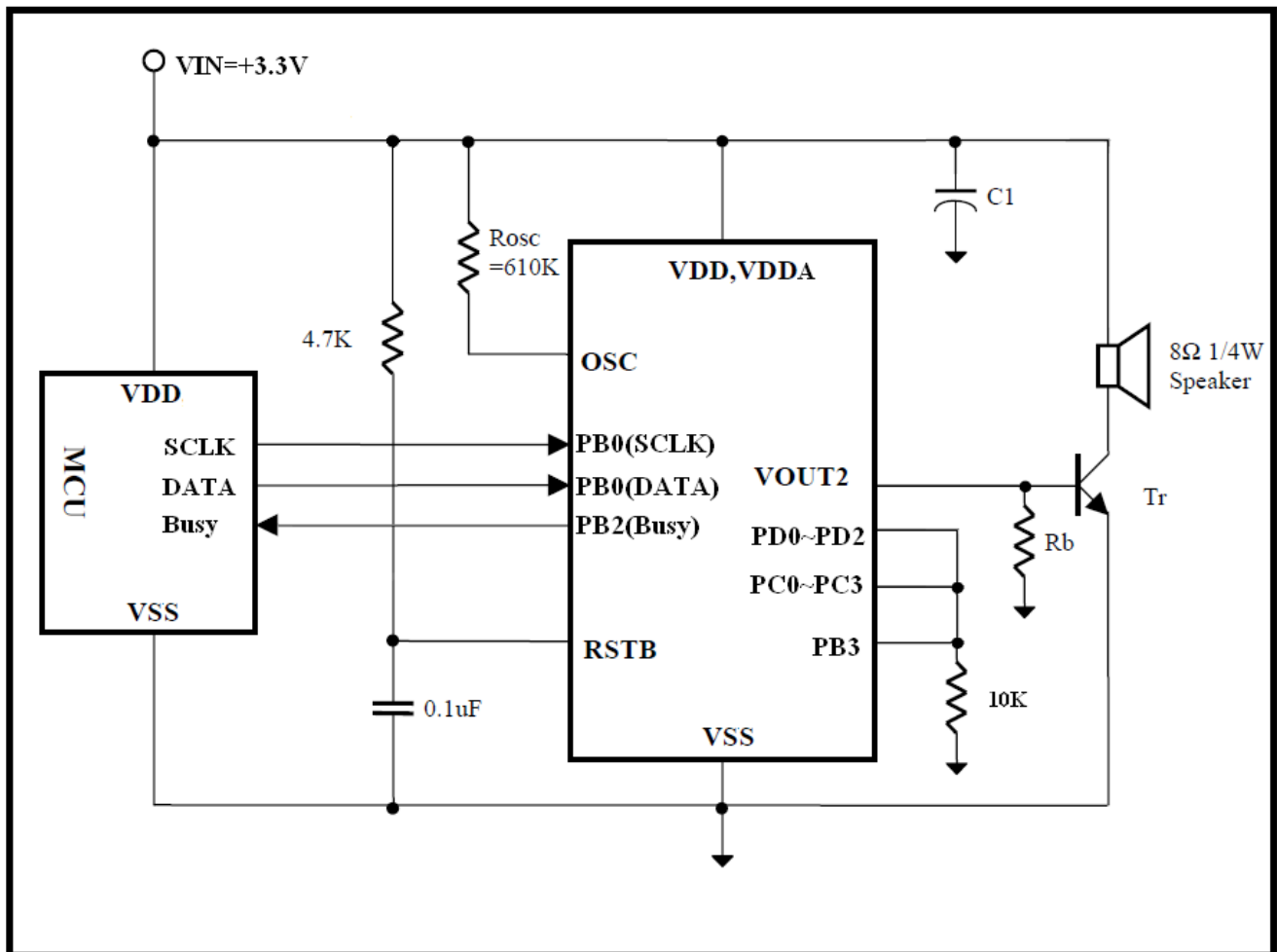
CPU Serial Mode

Symbol	Parameter	Min.	Typ.	Max	Unit
T_{SD}	Serial data stay / hold time	1	—	—	us
T_{RAMPH}	Ramp up time	—	—	64	ms
T_{RAMPL}	Ramp down time	—	—	64	ms
T_{BUSYH}	BUSY output set up time	—	—	1	ms
T_{BUSYL}	BUSY output set down time	—	—	1	ms

Note:

1) Ramp down from the value of the last sound sample. Max. time means ramp down from Voice data equal to FF(hex).

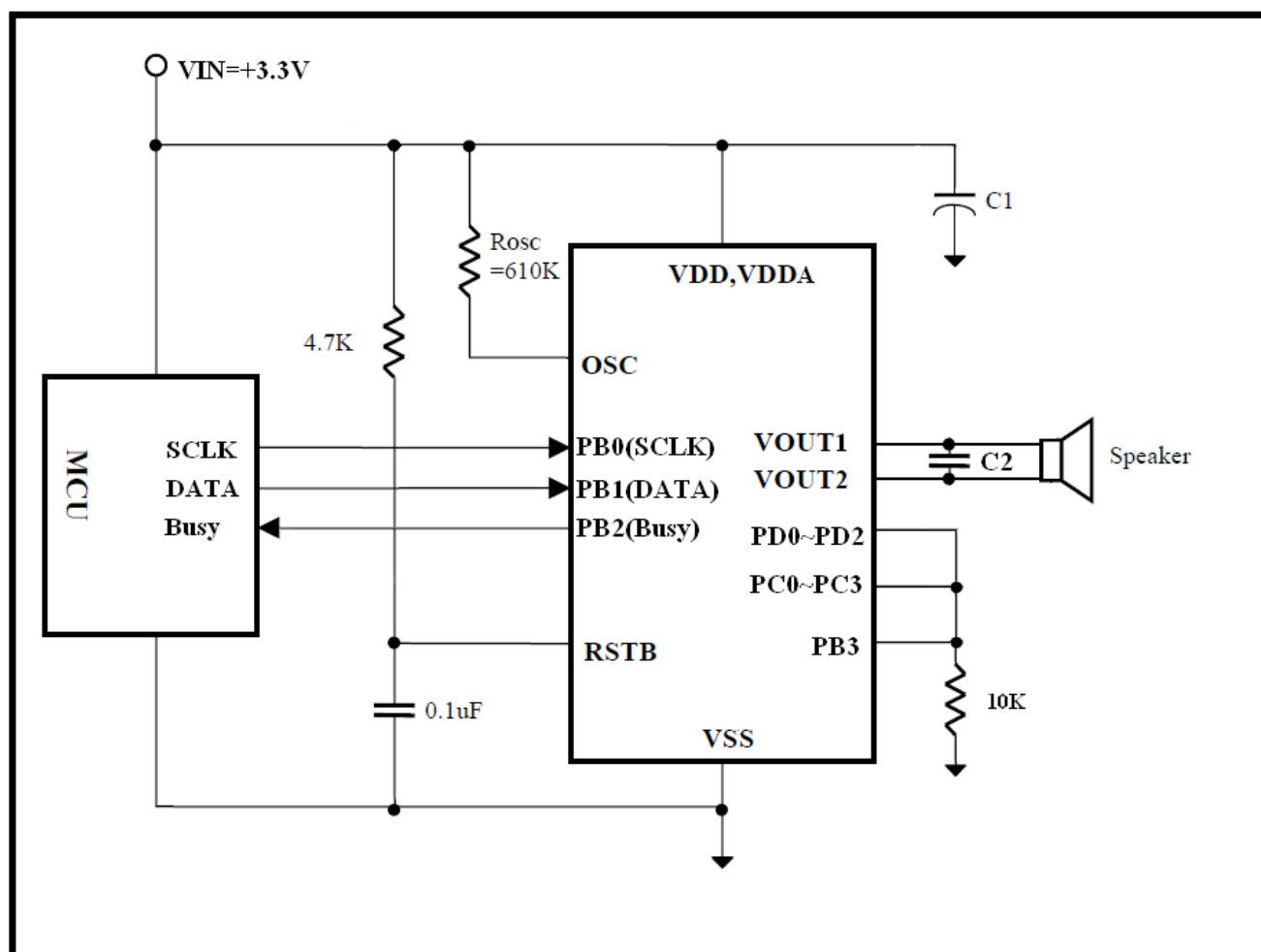
TYPICAL APPLICATIONS



Using 3.3V Battery with DAC speaker direct drive

Note

1. PB0 is serial clock pin (input) and it is set to internal pull-up.
2. PB1 is serial data pin (input) and it is set to internal pull-up.
3. PB2 is busy pin (output).
4. C1 must be connected directly on the VDD, VDDA, and VSS pins of the chip.



Using 3.3V Battery with PWM speaker direct drive

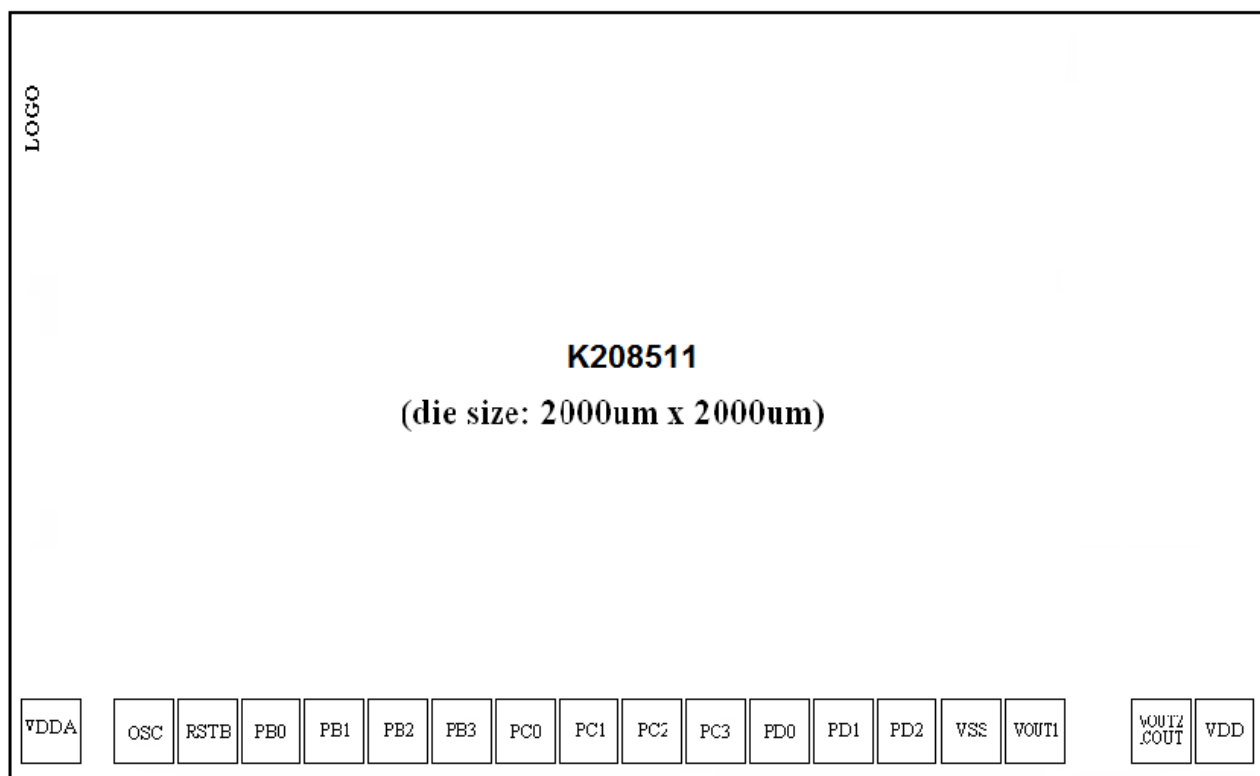
Note

1. PB0 is serial clock pin (input) and it is set to internal pull-up.
2. PB1 is serial data pin (input) and it is set to internal pull-up.
3. PB2 is busy pin (output).
4. C1 = 0.1uF to 2.2uF and placed before the main switch.
5. C2 is added according to the table below:

VOUT Volume	SPK	C2
Normal	8, 16 or 32 Ω	Not needed
High	16 or 32 Ω	Not needed
High	8 Ω	1000pF (102)
High	< 8 Ω	2000pF (202)



Bonding Diagrams



Note:

1. Substrate must be connected to VSS
2. Bonding pad size is 80 um x 80 um

Revision History

Date	Version	Changes
2012-11-21	V1.1	Create.