

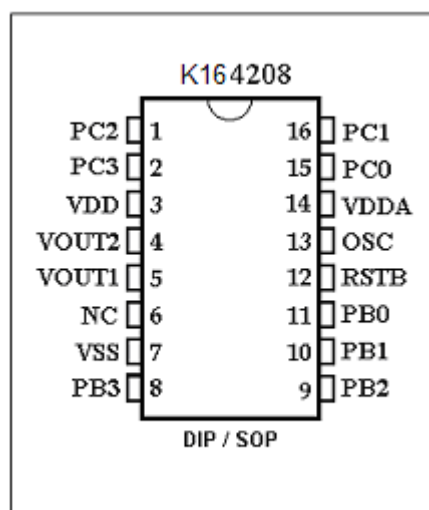


CPU Addressing Trigger without Output

FEATURES

- Addressing Mode Trigger
- Up to 128 voice groups
- Any combination of the trigger options:
 Level/Edge; Hold/Un-hold; Retrigger/Non-retrigger
- DAC through VOUT2_COUT pin
- PWM through VOUT1 and VOUT2
- No signal output supported
- Support 8-bit PCM, 5-bit uLaw and 4-bit ADPCM compression

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Pin Names	Description
VOUT1	PWM output to drive speaker directly
VOUT2_COUT	PWM output or COUT DAC output select by programmable option
OSC	Oscillator input
RSTB	Low active reset pin
VSS	Power Ground
VDD	Positive Power Supply
VDDA	Program power pin, connect to VDD during playback
PB0	TG Input trigger pin with internal pull-down
PB1~3, PC0~3	Address Input pins with internal pull-down

Pins for EPROM programming are: VDD, VDDA, VSS, PB0, PB1, OSC, VOUT2 and RSTB.



Ramp-up-down enable or disable

When COUT is used for playback, Ramp-up-down would be enabled. This function eliminates the 'POP' noise at the beginning and end of voice playback.

When VOUT1 and VOUT2 are used to drive speaker directly, the Ramp-up-down operation are disabled.

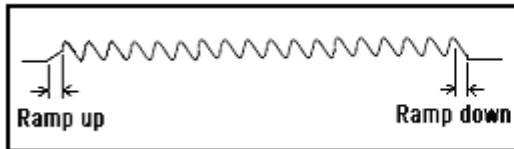


Fig. 1 Ramp-up-down Enable

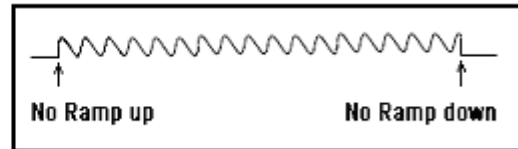


Fig.2 Ramp-up-down Disable

CPU Addressing Trigger Mode

In this mode, PB1, PB2, PB3, PC0, PC1, PC2 and PC3 are set to HIGH or LOW to provide the Group address for which the Group to be played. It is then followed by setting the PB0 input pin to HIGH, to strobe the Group address into the chip to start the actual playback.

PB1 = ADDR0 (least signification bit)

PB2 = ADDR1

...

PC3 = ADDR6 (most signification bit)

e.g. [ADDR6:ADDR0] = 0000000 => play Group #1

e.g. [ADDR6:ADDR0] = 0000100 => play Group #5

e.g. [ADDR6:ADDR0] = 1111111 => play Group #128

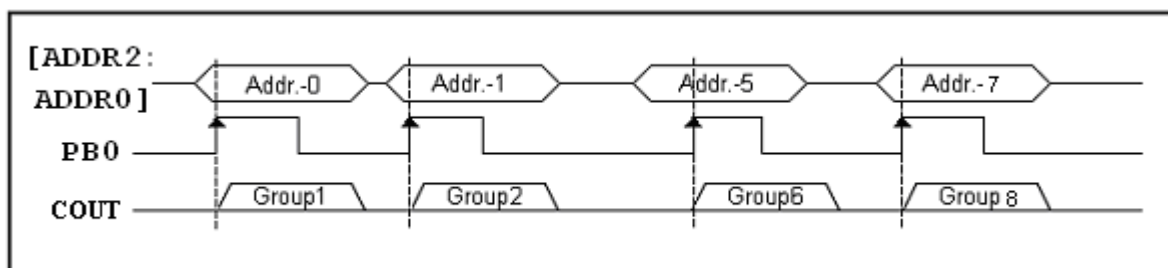


Fig. 3 CPU Address Trigger Mode

Trigger Options

User selectable options that affect each individual group are called Group Options. They are:

- Edge or Level trigger
- Unholdable or Holdable trigger
- Re-triggerable or non-retriggerable

Fig. 4 to Fig. 5 show the voice playback with different combination of triggering mode and the relationship between outputs and voice playback.

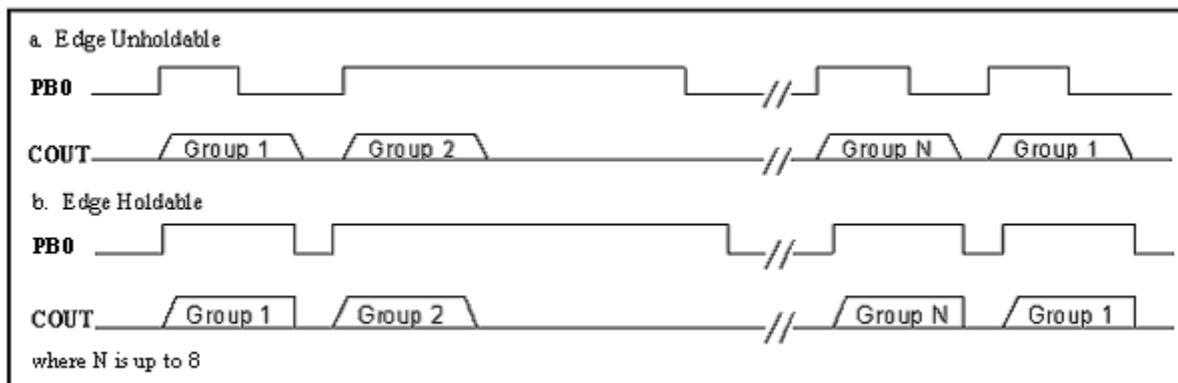


Fig. 4 Trigger with Edge Holdable and Unholdable option

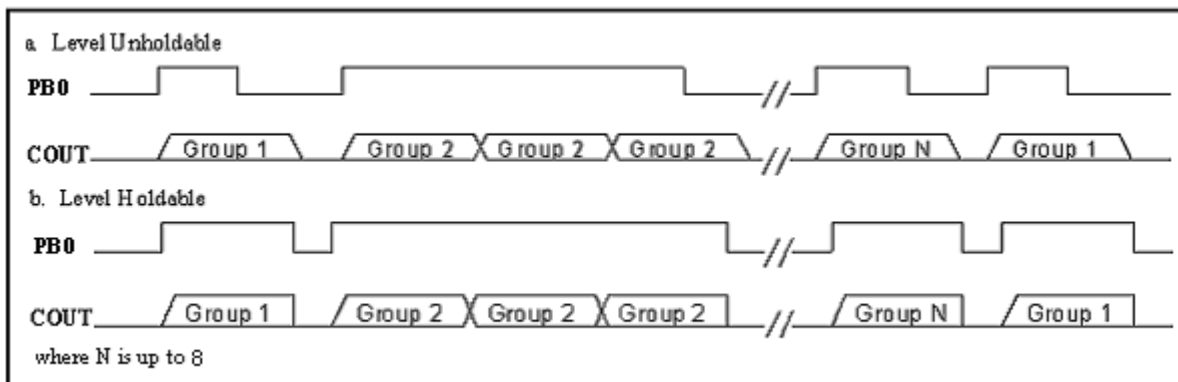
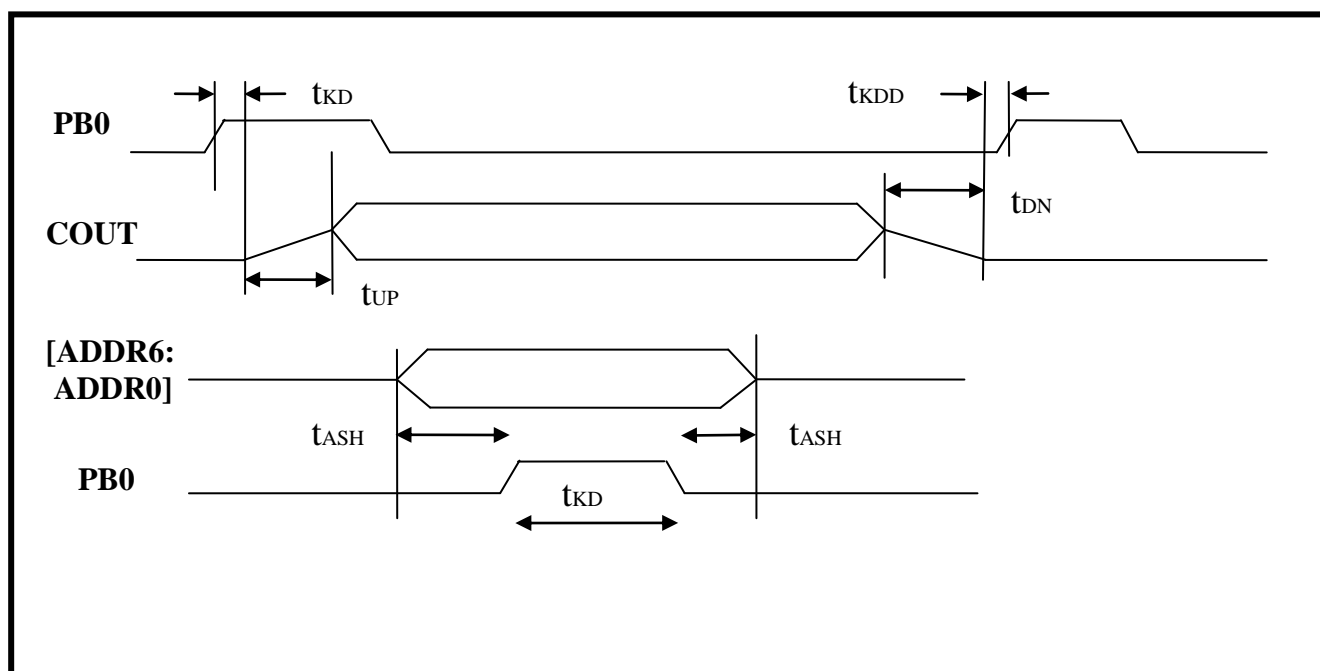


Fig. 5 Trigger with Level Holdable and Unholdable option



TRIGGER TIMING



Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
t _{KD}	Key trigger debounce time	64/F _s	—	—	sec	1
t _{UP}	Ramp up time	0	128/F _s	--	sec	1
t _{DN}	Ramp down time	0	--	256/F _s	sec	2
t _{ASH}	Address set-up / hold time	1/F _s	—	—	sec	
t _{KDD}	Key trigger delay after ramp down	--	0	--	ms	

Note:

1) Where F_s is sampling rate.

2) Ramp down is from the value of the last sound sample.

TYPICAL APPLICATIONS

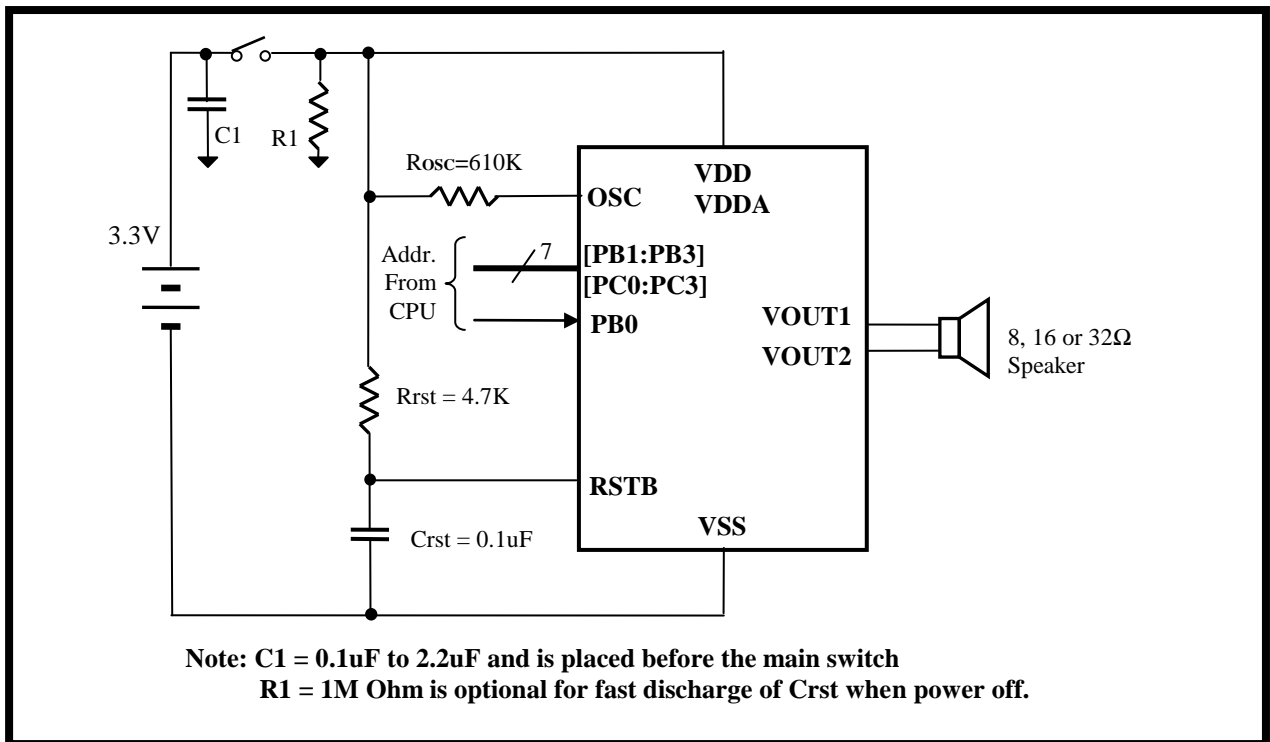


Fig 6. 3.3V Battery with PWM direct speaker drive

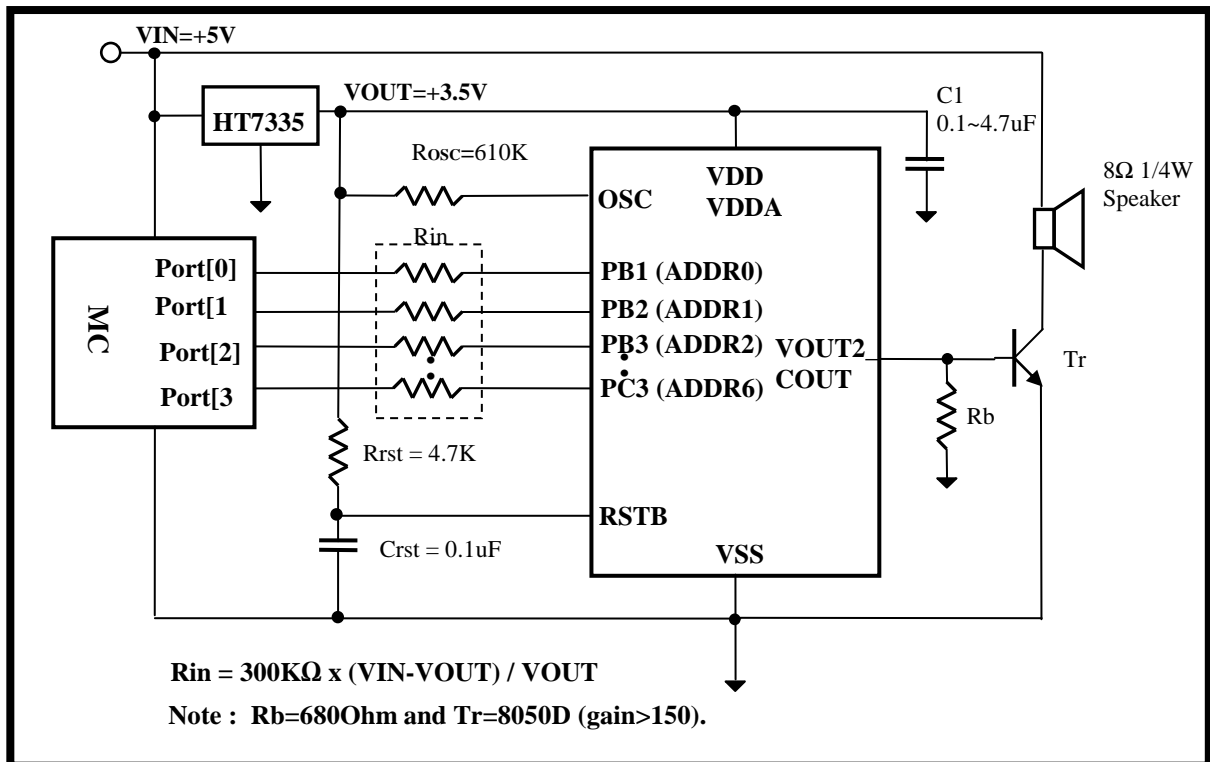
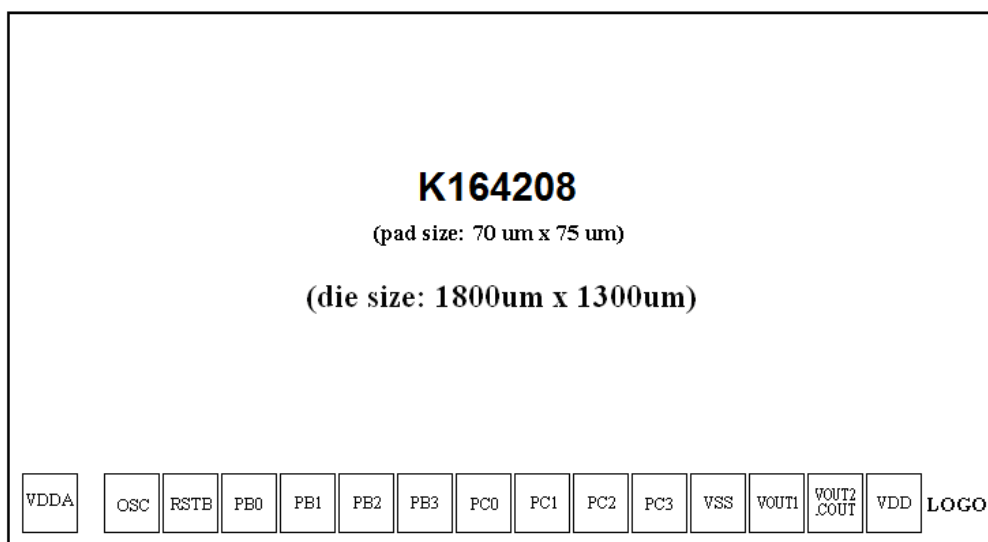


Fig 7. 5V Battery with Transistor direct drive



Bonding Diagrams



Note:

1. Substrate must be connected to VSS
2. Bonding pad size is 70 um x 75 um